IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (canceled), (withdrawn), (new), (previously presented), or (not entered). Please AMEND claims 1, 2, 5, 6, and 8-17 in accordance with the following:

1. (currently amended) An instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a storage circuit storing a combination of address mode information of a fetched instruction and an instruction address of the fetched instruction, after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

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a branch instruction control circuit controlling a branch instruction using the address mode information stored in the storage circuit after the fetched instruction is decoded in the decoding cycle if the fetched instruction is the branch instruction; and

a transfer circuit transferring the address mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed in an execution cycle of the instruction execution pipeline, the branch instruction control circuit controlling the branch instruction using the address mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change.

2. (currently amended) The instruction processing device according to claim 1, wherein said branch instruction control circuit stores a combination of the address mode information of ~~a~~ the branch destination of the branch instruction and an instruction address of the branch destination.

3. (original) The instruction processing device according to claim 2, wherein said branch instruction control circuit generates the address mode information of the branch destination based on the address mode information of the branch instruction.

4. (original) The instruction processing device according to claim 2, wherein said branch instruction control circuit judges whether address mode information and an instruction address of a branch destination predicted by a branch prediction are correct using the address mode information and instruction address of the branch destination.

5. (currently amended) The instruction processing device according to claim 2, wherein said branch instruction control circuit outputs a signal indicating the address mode information and instruction address of the branch destination when issuing a branch destination instruction fetch request to the instruction fetch pipeline.

6. (currently amended) The instruction processing device according to claim 1, wherein said branch instruction control circuit outputs a signal indicating whether the branch instruction is accompanied by ~~an~~ the address mode change when control of the branch instruction is terminated.

7. (original) The instruction processing device according to claim 1, further comprising a branch history circuit relating address mode information and an instruction address of a branch instruction to address mode information and an instruction address of a branch destination, storing related address mode information and instruction addresses of the branch instruction and branch destination, and making a branch prediction for the fetched branch instruction.

8. (currently amended) The instruction processing device according to claim 1,

further comprising a branch destination address generation circuit generating an instruction address of ~~a~~ the branch destination of the branch instruction using the address mode information stored in the storage circuit, and

wherein said transfer circuit transfers the address mode information stored in the storage circuit to the branch destination address generation circuit when the branch instruction is executed.

9. (currently amended) An instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a storage circuit storing a combination of mode information of a fetched instruction and an instruction address of the fetched instruction, after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

a branch instruction control circuit controlling a branch instruction using the mode information stored in the storage circuit after the fetched instruction is decoded in the decoding cycle if the fetched instruction is the branch instruction; and

a transfer circuit transferring the mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed in an execution cycle of the instruction execution pipeline, the branch instruction control circuit controlling the branch instruction using the mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by a mode change.

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10. (currently amended) An instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a fetch circuit fetching an instruction in the instruction fetch pipeline;

a storage circuit storing mode information of each fetched instruction as a part of an instruction address of the fetched instruction, after an instruction fetch request is issued and before each fetch instruction is decoded in a decoding cycle of the instruction execution pipeline; and

a control circuit controlling an instruction process of each instruction based on the ~~stored~~ mode information that has been stored, after the fetched instruction is decoded in the decoding cycle, the control circuit controlling a branch instruction using the mode information that has been stored as mode information of a branch destination of the branch instruction if the fetched instruction is the branch instruction and is not accompanied by a mode change.

11. (currently amended) An instruction processing device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

a plurality of storage ~~circuit~~ circuits, each storing a ~~plurality of combinations~~ combination of mode information of an instruction to be fetched and an instruction address of

the instruction, each combination stored in each storage circuit related to each of the plurality of instruction fetch ports; and

a fetch circuit performing an instruction fetch based on mode information corresponding to a first port ~~to be used~~ of the instruction fetch ports, performing an instruction pre-fetch of a branch destination of a branch instruction based on mode information corresponding to a second port of the instruction fetch ports, and continuing an instruction fetch based on the mode information corresponding to the second port if a branch is performed according to the branch instruction.

12. (currently amended) An instruction processing method using an instruction fetch pipeline and an instruction execution pipeline to perform an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

handling mode information of an information processing apparatus, which is to be determined when fetching each instruction, as a part of an instruction address;

fetching an instruction;

storing mode information of the fetched instruction as a part of an instruction address of the fetched instruction in each cycle of an instruction process for the fetched instruction, after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline; ~~and~~

controlling the instruction process for the fetched instruction based on the ~~stored~~ mode information that has been stored, after the fetched instruction is decoded in the decoding cycle, and when the fetched instruction is a branch instruction and is not accompanied by a mode change, using the mode information that has been stored as mode information of a branch destination of the branch instruction.

13. (currently amended) An instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

storage means for storing a combination of address mode information of a fetched instruction and an instruction address of the fetched instruction, after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

branch instruction control means for controlling a branch instruction using the address mode information stored in the storage means after the fetched instruction is decoded in the decoding cycle if the fetched instruction is the branch instruction; and

transfer means for transferring the address mode information stored in the storage means to the branch instruction control means when the branch instruction is executed in an execution cycle of the instruction execution pipeline, the branch instruction control means controlling the branch instruction using the address mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change.

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14. (currently amended) An instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

storage means for storing a combination of mode information of a fetched instruction and an instruction address of the fetched instruction, after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

branch instruction control means for controlling a branch instruction using the mode information stored in the storage means after the fetched instruction is decoded in the decoding cycle if the fetched instruction is the branch instruction; and

transfer means for transferring the mode information stored in the storage means to the branch instruction control means when the branch instruction is executed in an execution cycle of the instruction execution pipeline, the branch instruction control means controlling the branch instruction using the mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change.

15. (currently amended) An instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

fetch means for fetching an instruction;

storage means for storing mode information of each fetched instruction as a part of an instruction address of the fetched instruction, after an instruction fetch request is issued in

the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline; and

control means for controlling an instruction process of each instruction based on the ~~stored~~ mode information stored in the storage means, after the fetched instruction is decoded in the decoding cycle, the control means controlling a branch instruction using the mode information stored in the storage means as mode information of a branch destination of the branch instruction if the fetched instruction is the branch instruction and is not accompanied by a mode change.

16. (currently amended) An instruction processing device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

a plurality of storage means, each for storing a ~~plurality of combinations~~ combination of mode information of an instruction to be fetched and an instruction address of the instruction, each combination stored in each storage means related to each of the plurality of instruction fetch ports; and

fetch means for performing an instruction fetch based on mode information corresponding to a first port ~~to be used~~ of the instruction fetch ports, for performing an instruction pre-fetch of a branch destination of a branch instruction based on mode information corresponding to a second port of the instruction fetch ports, and for continuing an instruction fetch based on the mode information corresponding to the second port if a branch is performed according to the branch instruction.

17. (currently amended) An instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a storage circuit to store a combination of mode information and an instruction address for instructions to be fetched, after an instruction fetch request is issued in the instruction fetch pipeline and before a fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

a branch instruction control circuit to control execution of a branch instruction using the mode information stored in said storage circuit after one of the instructions to be fetched has been fetched as the branch instruction and decoded in the decoding cycle; and

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a transfer circuit to transfer the mode information stored in said storage circuit to said branch instruction control circuit when the branch instruction is executed in an execution cycle of the instruction execution pipeline, said branch instruction control circuit controlling the branch instruction using the address mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change.